What is claimed is:

1. A semiconductor device comprising:

an insulating layer;

an interconnection including a body of copper surrounded by said insulating layer;

a capping layer that covers said insulating layer, said capping layer having a window that exposes said interconnection; and

a metal resistor that extends along said capping layer and contacts a top surface of the interconnection through said window in the capping layer.

2. The device of claim 1, wherein the metal resistor is of a material selected from the group consisting of titanium, titanium nitride, tantalum, tantalum nitride, and tantalum silicon nitride.

3. The device of claim 2, wherein the metal resistor has a thickness of about 30 Å to 1000 Å.

4. The device of claim 1, wherein the capping layer is of a material selected from the group consisting of silicon nitride and silicon carbide.

5. A semiconductor device comprising:

an electrically conductive interconnection;

an insulating layer covering said interconnection;

an electrical contact that extends through said insulating layer and is electrically connected to the interconnection; and

a metal resistor extending on said insulating layer and contacting said electrical contact.

6. A semiconductor device comprising:

an insulating layer;

an interconnection including a body of copper surrounded by said insulating layer;

an MIM capacitor disposed on said insulating layer, said MIM capacitor including a lower electrode, a dielectric, and an upper electrode;

a capping layer that covers said insulating layer, said capping layer having a window that exposes said interconnection; and

a metal resistor that extends along said capping layer and contacts a top surface of the interconnection through said window in the capping layer, said metal resistor being of the same material as one of said lower electrode and said upper electrode of the MIM capacitor.

7. The device of claim 6, wherein said capping layer extends beneath said lower electrode of the MIM capacitor.

8. The device of claim 6, wherein said lower electrode of the MIM capacitor is surrounded by said insulating layer, and said capping layer extends between said upper electrode and said lower electrode so as to serve as said dielectric of the MIM capacitor.

9. A method of manufacturing a semiconductor device, the method comprising:

forming an insulating layer on a substrate;

forming a lower interconnection of copper layer within said insulating layer;

forming a capping layer on the insulating layer to cover and protect the lower interconnection;

forming a window in the capping layer to selectively expose a top surface of the lower interconnection; and

forming, on the capping layer, a metal resistor that contacts the top surface of the lower interconnection through the window.

10. The method of claim 9, wherein the forming of the lower interconnection comprises:

forming a trench in the insulating layer,

forming a copper layer on the insulating layer to fill the trench, and

planarizing the copper layer until a top surface of the insulating layer is exposed, whereby the lower interconnection is formed in the shape of the trench.

11. The method of claim 9, wherein said forming of the capping layer comprises forming one of a silicon nitride layer and a silicon carbide layer on the insulating layer.

12. The method of claim 9, wherein said forming of the metal resistor comprises forming a layer of a material selected from the group consisting of titanium, titanium nitride, tantalum, tantalum nitride, or tantalum silicon nitride on the insulating layer.

13. A method of manufacturing a semiconductor device, the method comprising:

forming an insulating layer on a substrate;

forming a first lower interconnection and a second lower interconnection, of copper, within the insulating layer;

forming a capping layer on the insulating layer to cover and protect the first lower interconnection and the second lower interconnection;

forming a window in the capping layer to selectively expose a top surface of the first lower interconnection;

forming, on the capping layer, a metal resistor in contact with the top surface of the first lower interconnection through the window;

forming a second insulating layer over the metal resistor;

forming an electrical contact that extends through the second insulating layer and into contact with the second lower interconnection; and

forming an upper interconnection electrically connected to the electrical contact.

14. The method of claim 13, wherein said forming of the electrical or upper interconnection comprises forming a copper layer using a damascene process.

15. A method of manufacturing a semiconductor device, the method comprising:

forming an insulating layer on a substrate;

forming a first lower interconnection and a second lower interconnection of copper within the insulating layer;

forming a capping layer on the insulating layer to cover and protect the first lower interconnection and the second lower interconnection;

forming a window in the capping layer to selectively expose a top surface of the first lower interconnection;

forming, on the capping layer, a metal layer that contacts the top surface of the first lower interconnection through the window;

patterning the metal layer to form therefrom a metal electrode of a MIM capacitor and a metal resistor that contacts the first lower interconnection through the window;

forming a second insulating layer over the metal resistor and the metal electrode of the MIM capacitor; and

forming a connection contact body penetrating the second insulating layer to contact the second lower interconnection and forming an upper interconnection electrically connected to the connection contact body.

16. The method of claim 15, wherein said patterning of the metal layer forms an upper electrode of the MIM capacitor.

17. The method of claim 16, and further comprising forming a lower electrode, which is disposed under the capping layer and is opposed to the upper electrode, such that the capping layer serves as the dielectric of the MIM capacitor.

18. The method of claim 17, wherein the lower electrode is formed at the same time as the first lower interconnection and the second lower interconnection.

19. The method of claim 16, and further comprising forming a lower electrode on the capping layer and opposed to the upper electrode, and forming a dielectric layer on the lower electrode.

20. The method of claim 15, wherein said patterning of the metal layer forms a lower electrode of the MIM capacitor.

21. The method of claim 20, and further comprising forming a dielectric layer on the lower electrode, and forming an upper electrode on the dielectric layer and opposed to the lower electrode.

22. A method of manufacturing a semiconductor device, the method comprising:

forming an insulating layer on a substrate;

forming a first lower interconnection, a second lower interconnection, and a third lower interconnection of copper within the insulating layer;

forming a capping layer on the insulating layer to cover and protect the first lower interconnection, the second lower interconnection, and the third lower interconnection;

forming a first window in the capping layer to selectively expose a top surface of the first lower interconnection;

forming, on the capping layer, a lower electrode layer comprising a metal in contact with the top surface of the first lower interconnection through the first window;

patterning the lower electrode layer to form a lower electrode of an MIM capacitor, and a first metal resistor that contacts the first lower interconnection through the first window;

forming a dielectric layer over the first metal resistor and the first lower electrode;

forming a second window in the dielectric layer and the capping layer to selectively expose a top surface of the second lower interconnection;

forming, on the dielectric layer, an upper electrode layer comprising a metal that contacts the top surface of the second lower interconnection through the second window;

patterning the upper electrode layer to form an upper electrode opposed to the lower electrode, and a second metal resistor that contacts the second lower interconnection through the second window;

forming a second insulating layer over the second metal resistor and the upper electrode;

forming an electrical contact that extends through the second insulating layer into contact with the third interconnection; and

forming an upper interconnection electrically connected to the electrical contact.

23. A method of manufacturing a semiconductor device, the method comprising:

forming an interconnection;

forming an insulating layer over the interconnection;

forming an electrical contact that extends through the insulating layer and is electrically connected to the interconnection; and

forming a metal resistor on the insulating layer in contact with the electrical contact.

24. The method of claim 23, wherein said forming of the electrical contact comprises forming a layer of copper in the insulating layer.

25. The method of claim 24, and further comprising forming, on the insulating layer, a capping layer that covers and protects a surface of the copper electrical contact; and subsequently forming a window in the capping layer to expose the surface of the copper electrical contact.